Amendments to the Specification

Please replace the paragraph that begins at page 4, line 33 with the following amended paragraph.

In particular, the analog interface 40 includes, for each of ~~the~~ red, green and blue analog display signals 56, an analog-to-digital converter (ADC) 42 coupled between a clamp 41 and a data formatter 43. It further includes a phase-locked loop (PLL) 44, a pixel clock synthesizer 46, a clock controller 50 and an associated memory 48, a clamp generator 52 and an offset and gain adjuster 54.

Please replace the paragraph that begins at page 5, line 22 with the following amended paragraph.

The pixel clock synthesizer 46 introduces a phase shift (e.g., a delay) to position the reference signal and thereby form a sample clock which drives wide-band samplers 47 in each of the ADCs 42. In response to the red, green and blue analog display signals 56 and to the sample clock, the samplers provide analog samples which are then quantized by the converter portions of the ADCs 42. Finally, the data formatters 43 convert the quantized signals into formats compatible with the graphics controller 34.